Electronic Version
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Claims

[c1] A method of fabricating a semiconductor device structure, comprising:
providing a substrate;
providing an electrode on the substrate;
forming a recess in the electrode, the recess having an opening;
disposing a small grain semiconductor material within the recess;
covering the opening to contain the small grain semiconductor material within the recess, and then
annealing the resultant structure

[c2] The method is claimed in claim 1, wherein said step of annealing includes annealing the resultant structure at an approximately constant temperature in a range of about 500^{o}C to about 600^{o}C for about one hour.

[c3] The method as claimed in claim 1, wherein the small grain semiconductor material is a polysilicon material having an average grain diameter in a range of approximately one nm to approximately 30 nm.

[c4] The method as claimed in claim 1, wherein said step of

covering includes masking the entire opening.

[c5] A semiconductor device structure, comprising:
a first semiconductor device having a first gate stack, and
a second semiconductor device having a second gate stack; wherein said first gate stack includes a first semiconductor material having an average grain size of less than approximately 30nm, and wherein said second gate stack includes a second semiconductor material having an average grain size of greater than approximately 30nm.

[c6] The structure as claimed in claim 5, wherein said first semiconductor material is a grained polysilicon.

[c7] The structure as claimed in claim 5, wherein said first semiconductor device is an nFET and said second semiconductor device is a pFET.

[c8] The structure as claimed in claim 5, further comprising a first channel disposed below said first gate stack, and a second channel disposed below said second gate stack; wherein the second gate stack imparts a compressive stress to the second channel in a range of approximately -200MPa to approximately -600MPa, while the first gate stack imparts a compressive stress to the first channel in

a range of approximately -10 MPa to approximately -100 MPa.

[c9] The structure as claimed in claim 5, further comprising an isolation region disposed between said first semiconductor device and said second semiconductor device.

[c10] The structure as claimed in claim 5, wherein said second semiconductor material is a grained polysilicon.

[c11] The structure as claimed in claim 5, further comprising a third semiconductor material and a fourth semiconductor material, wherein said first semiconductor material is disposed on said third semiconductor material and wherein said second semiconductor material is disposed on said fourth semiconductor material.

[c12] The structure as claimed in claim 11, wherein said third semiconductor material is a small grained polysilicon and said fourth semiconductor material is a small grained polysilicon.

[c13] A method for fabricating a semiconductor device structure, comprising:
providing a substrate;
forming an nFET and a pFET on the substrate;
replacing portions of the gate electrodes from the nFET and said pFET with a small-grained polysilicon;

covering the small-grained polysilicon of the nFET, and then heating the nFET and the pFET, so that an average diameter of the grains within the nFET is less than an average diameter of the grains within the pFET.

[c14] The method as claimed in claim 13, wherein said step of heating includes heating the nFET and the pFET to temperatures within a range of approximately 500°C to approximately 600° C for approximately one hour.

[c15] The method as claimed in claim 13, wherein the small-grained polysilicon has an average grain size in a range of about five nm to about 30nm.

[c16] The method as claimed in claim 13, wherein said step of replacing includes removing the portions of the gate electrodes to form recesses, and then disposing the grained polysilicon within the nFET and pFET recesses.

[c17] The method as claimed in claim 13, wherein said step of replacing includes removing the entire portions of the gate electrodes to form recesses, and then depositing the small-grained polysilicon within the recesses.

[c18] The method as claimed in claim 13, wherein said step of covering includes disposing a mask over the grained polysilicon of the nFET, the mask consisting essentially of SiN.

[c19] The method as claimed in claim 13, further comprising forming spacers for the
nFET and the pFET, the spacers having different heights.

[c20] The method as claimed in claim 13, further comprising providing spacers for the nFET and the pFET, the spacers for the pFET having heights which are less than heights of the spacers for the nFET.